1. A method for selecting a placement of misfit dislocations, the method comprising the steps of:

forming a first layer over a substrate, the first layer having a first equilibrium lattice constant; and

forming a second layer over the first layer, the second layer having (i) a second equilibrium lattice constant different from the first equilibrium lattice constant, and (ii) a critical thickness at which a plurality of misfit dislocations form at an interface proximate the second layer,

wherein a thickness of the second layer is selected to define a distance between a top surface of the second layer and the misfit dislocations that form at the interface corresponding to the selected placement of misfit dislocations when the thickness is equal to or greater than the critical thickness.

2. The method of claim 1, wherein the first layer comprises a relaxed layer.

3. The method of claim 1, wherein the first layer comprises a compressively strained layer.

4. The method of claim 1, wherein the first layer comprises germanium.

5. The method of claim 1, wherein the second layer comprises a tensilely strained layer.

6. The method of claim 1, wherein the second layer comprises a compressively strained layer.

7. The method of claim 1, wherein the second layer comprises silicon.

8. The method of claim 1, wherein the thickness of the second layer is selected to reduce carrier recombination.

9. The method of claim 1, further comprising:

introducing a plurality of dopants into a portion of the first layer,

wherein the thickness of the second layer is selected to reduce lateral diffusion piping of the dopants along the interface between the first layer and second layers.

10. The method of claim 1, further comprising:

defining at least one of a source and a drain region by introducing a plurality of dopants into a portion of the second layer,

wherein a bottommost portion of the source or drain region is disposed at a preselected distance from the misfit dislocations at the interface.

11. The method of claim 10, wherein the preselected distance is selected so that the source or drain is substantially free of misfit dislocations.

12. The method of claim 11, wherein the bottommost portion of the source or drain region is disposed above the interface.

13. The method of claim 11, wherein the thickness of the second layer is at least 1000 Å.

14. The method of claim 11, wherein the at least one of the source and the drain regions comprises an extension, and the misfit dislocations at the interface are disposed (i) below the extension and (ii) above the bottommost portion of the source or drain region.

15. The method of claim 14, wherein the thickness of the second layer is selected from the range comprising approximately 400 angstroms to 500 angstroms.

16. The method of claim 10, wherein defining the source or drain region comprises the introduction of the plurality of dopants by a single implantation step.

17. The method of claim 10, wherein at least one source and at least one drain are formed and the source and the drain regions cooperate to form a transistor.

18. The method of claim 10, further comprising:

forming a semiconductor layer over a portion of the second layer,

wherein at least a portion of the semiconductor layer is disposed over the source or drain region.

19. The method of claim 18, wherein the semiconductor layer comprises a material selected from the group consisting of a group II, a group III, a group IV, a group V, a group VI element, and combinations thereof.

20. The method of claim 18, wherein a thickness of the semiconductor layer is selected so that the bottommost portion of the source or drain region is disposed above the preselected distance from the interface.

21. The method of claim 18, further comprising:

forming a metal layer over the semiconductor layer; and

heating the substrate to form a contact layer including metal-semiconductor alloy, the contact layer comprising at least a portion of the semiconductor layer and at least a portion of the metal layer.

22. The method of claim 21, wherein forming the contact layer comprises consuming substantially all of the semiconductor layer.

23. The method of claim 21, wherein forming the contact layer comprises consuming at least a portion of the second layer.

24. The method of claim 21, wherein forming the contact layer comprises consuming only a portion of the semiconductor layer.

25. The method of claim 21, wherein the semiconductor layer has a third equilibrium constant, and the third equilibrium constant is substantially equal to the first equilibrium constant of the first layer.

26. A method for forming a semiconductor structure, the method comprising the steps of:

forming a first layer over a substrate, the first layer having a first equilibrium lattice constant; and

forming a second layer over the first layer, the second layer having (i) a second equilibrium lattice constant different from the first equilibrium lattice constant, and (ii) a critical

thickness at which a plurality of misfit dislocations form at an interface proximate the second layer,

wherein a thickness of the second layer is selected to define a distance between a top surface of the second layer and the misfit dislocations that form at the interface such that a device formed over the second layer has an off current less than approximately 10^{-8} Amperes/micrometer and a strained channel.

27. A method for placing misfit dislocations at a desired location within a semiconductor structure, the method comprising the steps of:

forming a first layer over a substrate, the first layer comprising a first material having a first equilibrium lattice constant;

forming a second layer over the first layer, the second layer comprising a second material having (i) a second equilibrium lattice constant different from the first equilibrium lattice constant, and (ii) a critical thickness at which a plurality of misfit dislocations form at an interface proximate the second layer; and

selecting the first material, the second material, and a second layer thickness to place the misfit dislocations at the desired location.

28. A semiconductor structure having a selected placement of misfit dislocations, the structure comprising:

a first layer disposed over a substrate, the first layer having a first equilibrium lattice constant; and

a second layer disposed over the first layer, the second layer having (i) a second equilibrium lattice constant different from the first equilibrium lattice constant, and (ii) a critical thickness at which a plurality of misfit dislocations form at an interface proximate the second layer,

wherein a thickness of the second layer is selected to define a distance between a top surface of the second layer and the misfit dislocations that form at the interface corresponding to the selected placement when the thickness is equal to or greater than the critical thickness.

29. The structure of claim 28, wherein the first layer comprises a relaxed layer.

30. The structure of claim 28, wherein the first layer comprises a compressively strained layer.

31. The structure of claim 28, wherein the first layer comprises germanium.

32. The structure of claim 28, wherein the second layer comprises a tensilely strained layer.

33. The structure of claim 28, wherein the second layer comprises silicon.

34. The structure of claim 28, wherein the thickness of the second layer is selected to reduce carrier recombination.

35. The structure of claim 28, further comprising:

a plurality of dopants disposed in a portion of the first layer,

wherein the thickness of the second layer is selected to reduce diffusion piping of the dopants out of the portion of the first layer.

36. The semiconductor structure of claim 28, further comprising:

a transistor formed over the second layer, the transistor including:

(i) a gate dielectric disposed over a portion of the second layer,

(ii) a gate disposed over the gate dielectric, the gate comprising a conducting material, and

(iii) a source and a drain disposed proximate the gate and extending into the second layer,

wherein the misfit dislocations are disposed at a preselected distance from an interface between the gate dielectric and the second layer.

37. The structure of claim 36, wherein the transistor has an off current of less than 10^{-8} Amperes/micrometer and a strained channel.

38. The structure of claim 28, further comprising:

at least one of a source and a drain region defined in a portion of the second layer and comprising a plurality of dopants,

wherein the second layer has a thickness greater than the critical thickness and a bottommost portion of the source or drain region is disposed at a preselected distance from the misfit dislocations at the interface.

39. The structure of claim 38, wherein the first layer comprises a relaxed layer.

40. The structure of claim 38, wherein the first layer comprises a compressively strained layer.

41. The structure of claim 38, wherein the first layer comprises germanium.

42. The structure of claim 38, wherein the second layer comprises a tensilely strained layer.

43. The structure of claim 38, wherein the second layer comprises a compressively strained layer.

44. The structure of claim 38, wherein the second layer comprises silicon.

45. The structure of claim 38, wherein the preselected distance is selected so that the source or drain region is substantially free of misfit dislocations.

46. The structure of claim 38, wherein substantially all of the bottommost portion of the source or drain region is substantially equidistant from a topmost portion of the source or drain region disposed in the second layer.

47. The structure of claim 38, wherein the at least one source or drain comprises a source and a drain, and the source and the drain regions cooperate to form a transistor.

48. The structure of claim 38, further comprising:

a contact layer including a metal-semiconductor alloy disposed over a portion of the second layer.

49. The structure of claim 48, wherein the contact layer extends into the portion of the second layer.

50. The structure of claim 38, further comprising:

a semiconductor layer disposed over the portion of the second layer,

wherein a portion of the source or drain region is disposed in the semiconductor layer.

51. The structure of claim 50, wherein the semiconductor layer comprises a material selected from the group consisting of a group II, a group III, a group IV, a group V, a group VI element, and combinations thereof.

52. The structure of claim 50, wherein the semiconductor layer has a third equilibrium lattice constant substantially equal to the first equilibrium lattice constant.

53. The structure of claim 50, further comprising:

a contact layer including a metal-semiconductor alloy disposed over the semiconductor layer.

54. A semiconductor structure comprising:

a first layer disposed over a substrate, the first layer having a first equilibrium lattice constant; and

a second layer disposed over the first layer, the second layer having (i) a second equilibrium lattice constant different from the first equilibrium lattice constant, and (ii) a critical thickness at which a plurality of misfit dislocations form at an interface proximate the second layer,

wherein a thickness of the second layer is selected to define a distance between a top surface of the second layer and the misfit dislocations that form at the interface such that a device formed over the second layer has an off current less than approximately 10^{-8} Amperes/micrometer and a strained channel.

55. A method for selecting a placement of misfit dislocations, the method comprising the steps of:

forming a first layer portion over a substrate, the first layer having a first equilibrium lattice constant;

forming a regrowth layer over the first layer portion, the regrowth layer having a regrowth equilibrium lattice constant different from the first equilibrium lattice constant, wherein

a plurality of misfit dislocations form at an interface between the first layer portion and the regrowth layer;

forming a second layer over the regrowth layer; and

selecting a thickness of the regrowth layer to define a distance between a top surface of the second layer and the misfit dislocations corresponding to the selected placement of the misfit dislocations.

56. The method of claim 55, wherein the second layer is strained.

57. The method of claim 55, wherein a lattice mismatch between the first equilibrium lattice constant and the regrowth layer is less than about 0.04%,

58. The method of claim 57, wherein the thickness of the regrowth layer is less than about 450 nanometers.

59. The method of claim 57, wherein the first layer comprises a first germanium content, the regrowth layer comprises a second germanium content, and the difference between the first germanium content and the second germanium content is less than about 1%.

60. The method of claim 55, wherein a lattice mismatch between the first equilibrium lattice constant and the regrowth layer is less than about 0.08%.

61. The method of claim 60, wherein the thickness of the regrowth layer is less than about 210 nanometers.

62. The method of claim 60, wherein the first layer comprises a first germanium content, the regrowth layer comprises a second germanium content, and the difference between the first germanium content and the second germanium content is less than about 2%.

63. The method of claim 55, wherein a lattice mismatch between the first equilibrium lattice constant and the regrowth layer is less than about 0.12%.

64. The method of claim 63, wherein the thickness of the regrowth layer is less than about 130 nanometers.

65. The method of claim 63, wherein the first layer comprises a first germanium content, the regrowth layer comprises a second germanium content, and the difference between the first germanium content and the second germanium content is less than about 3%.

66. A method for suppressing the formation of misfit dislocations, the method comprising the steps of:

forming a first layer portion over a substrate, the first layer having a first equilibrium lattice constant and a first composition; and

forming a regrowth layer over the first layer portion, the regrowth layer having a regrowth equilibrium lattice constant and a regrowth composition,

wherein the formation of misfit dislocations at an interface between the first layer portion and the regrowth layer is suppressed by the selection of the first and regrowth equilibrium lattice constants and the first and regrowth compositions.

67. The method of claim 66, wherein the regrowth equilibrium lattice constant is substantially identical to the first equilibrium lattice constant.

68. The method of claim 66, wherein the regrowth composition is substantially identical to the first layer portion composition.

69. The method of claim 66, further comprising:

growing a second layer over the regrowth layer.

70. The method of claim 69, wherein the second layer is strained.

71. A semiconductor structure comprising:

a first layer portion disposed over a substrate, the first layer having a first equilibrium lattice constant;

a regrowth layer disposed over the first layer portion, the regrowth layer having a regrowth equilibrium lattice constant different from the first equilibrium lattice constant; and

a second layer disposed over the regrowth layer,

wherein a plurality of misfit dislocations are disposed at an interface between the first layer portion and the regrowth layer, and the regrowth layer has a thickness selected to define a distance between a top surface of the second layer and the misfit dislocations.

72. The structure of claim 71, wherein the second layer is strained.

73. A semiconductor structure comprising:

a first layer portion disposed over a substrate, the first layer having a first equilibrium lattice constant; and

a regrowth layer disposed over the first layer portion, the regrowth layer having a regrowth equilibrium lattice constant substantially identical to the first equilibrium lattice constant,

wherein a density of misfit dislocations disposed at an interface between the first layer portion and the regrowth layer is substantially zero per square centimeter.

74. The structure of claim 73, further comprising:

a second layer disposed over the regrowth layer.

75. The structure of claim 74, wherein the second layer is strained.

76. A method for selecting a placement of a dislocation array, the method comprising:

providing a substrate having a first equilibrium lattice constant;

forming a first layer over the substrate, the first layer having a second equilibrium lattice constant; and

selecting a thickness of the first layer to define a distance between a top surface of the first layer and an interface between the first layer and the substrate,

wherein a dislocation array is disposed at the interface corresponding to the selected placement of the dislocation array.

77. The method of claim 76, wherein the first layer is strained.

78. The method of claim 76, wherein the first equilibrium lattice constant is substantially identical to the second equilibrium constant, a composition of the first layer is substantially identical to a composition of the substrate.

79. A method for selecting a placement of a dislocation array, the method comprising:

providing a substrate having a first equilibrium lattice constant;

forming a first layer over the substrate, the first layer having a second equilibrium lattice constant; and

selecting a thickness of the first layer to define a distance between a top surface of the first layer and an interface between the first layer and the substrate,

wherein the misfit dislocations form at the interface and the thickness of the first layer is selected such that a device formed over the first layer has an off current less than 10^{-8} Amperes/micrometer and a strained channel.

80. A semiconductor structure comprising:

a substrate having a first equilibrium lattice constant; and

a first layer disposed over the substrate, the first layer having a second equilibrium lattice constant;

wherein a thickness of the first layer is selected to define a distance between a top surface of the first layer and an interface between the first layer and the substrate, a dislocation array is disposed at the interface, and the thickness of the first layer provides (i) an off current less than 10^{-8} Amperes/micrometer and (ii) a strained channel in a device formed over the first layer.

81. The semiconductor structure of claim 80, further comprising:

a transistor formed over the first layer, the transistor including:

(i) a gate dielectric disposed over a portion of the first layer,

(ii) a gate disposed over the gate dielectric, the gate comprising a conducting material, and

(iii) a source and a drain disposed proximate the gate and extending into the first layer,

wherein the dislocation array is disposed at a preselected distance from an interface between the gate dielectric and the first layer.

82. A semiconductor structure having a selected placement of a dislocation array, the structure comprising:

a substrate having a first equilibrium lattice constant; and

a first layer disposed over the substrate, the first layer having a second equilibrium lattice constant;

wherein a thickness of the first layer is selected to define a distance between a top surface of the first layer and the dislocation array that forms at the interface corresponding to the selected placement.

83. The semiconductor structure of claim 82, further comprising:

a transistor formed over the first layer, the transistor including:

(i) a gate dielectric disposed over a portion of the first layer,

(ii) a gate disposed over the gate dielectric, the gate comprising a conducting material, and

(iii) a source and a drain disposed proximate the gate and extending into the first layer,

wherein the dislocation array is disposed at a preselected distance from an interface between the gate dielectric and the first layer.